



UNITED STATES PATENT AND TRADEMARK OFFICE

20h

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/787,487	02/26/2004	Lawrence A. Clevenger	YOR920010565US2	4987
29154	7590	06/30/2005	EXAMINER	
FREDERICK W. GIBB, III MCGINN & GIBB, PLLC 2568-A RIVA ROAD SUITE 304 ANNAPOLIS, MD 21401			THOMAS, TONIAE M	
			ART UNIT	PAPER NUMBER
			2822	

DATE MAILED: 06/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/787,487

Applicant(s)

CLEVINGER ET AL.

Examiner

Toniae M. Thomas

Art Unit

2822

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 26 February 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 11-23 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 11-23 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 26 February 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>02/26/04; 05/12/05</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. This is a first Office action on the merits of Application Serial No. 10/787,487, which is a divisional of Application Serial No. 10/224,899 filed on 21 August 2002, now US Patent No. 6,787,836.
2. The preliminary amendment filed on 26 February 2004 canceled claims 1-10. Accordingly, claims 11-23 are pending.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 11-19 are rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for *a second metal layer comprising a gate of the transistor and a plate of the capacitor*, does not reasonably provide enablement for *a second metal layer comprising a gate of the transistor and a plate of the transistor*, as recited in claims 11 and 19 (claim 11, lines 7-8; claim 19, lines 11-12). The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make the invention commensurate in scope with these claims. Claims 11 and 19 both recite the limitation *wherein said second metal layer comprises a gate of said transistor and a plate of said transistor* (claim 11, lines 7-8; claim 19, lines 11-12). However, the disclosure clearly describes a second metal layer, which is

Art Unit: 2822

patterned to form transistor gates and capacitor plates (see fig. 11 and page 9, par. 33).

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 13 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The phrase *said sidewall spacers lacks* antecedent basis.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 11, 13, and 16-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Moriwaki et al. (US 6,333,223 B1).

Insofar as in compliance with 35 USC 112, first paragraph, the Moriwaki et al. patent (Moriwaki) discloses a method of forming a capacitor and an associated semiconductor transistor having a metal gate [figs. 7(a)-9(b) and

accompanying text). The method comprises: forming a first metal layer 303 [fig. 7(a) and col. 11, lines 47-63]; forming an insulator 307 over the first metal layer [fig. 7(a) and col. 12, lines 5-9]; removing a portion of the first metal layer 303 from a gate region [fig. 8(b) and col. 12, lines 23-32]; and forming a second metal layer 313, 314 over the insulator and in the gate region [fig. 9(a) and col. 12, lines 35-42], wherein the second metal layer comprises a gate 320 of the transistor and a plate 323 of the capacitor [fig. 9(b) and col. 12, lines 43-61].

Source and drain regions 306 are doped in said substrate after forming sidewall spacers 305 [fig. 7(a) and col. 11, line 66 - col. 12, line 5].

An insulator 312 is formed over the first metal layer [fig. 9(a) and col. 12, lines 33-35].

The insulator comprises both a capacitor insulator 321 and a gate insulator 318 [fig. 9(b) and col. 12, lines 43-61].

The plate 323 comprises an upper plate of the capacitor [fig. 9(b) and col. 12, lines 59-61].

Allowable Subject Matter

6. Claim 19 would be allowable if rewritten or amended to overcome the rejection under 35 U.S.C. 112, first paragraph, set forth in this Office action. Likewise, dependent claims 20-23 would be allowable if rewritten to overcome the rejection under 35 U.S.C. 112, first paragraph, set forth in this Office action and to include all of the limitations of the base claim, claim 19, and any intervening claims. The prior art of record does not anticipate, teach or

Art Unit: 2822

suggest a method of forming a capacitor and an associated transistor substantially as claimed, wherein the method comprises: patterning sacrificial gate structures over a substrate, forming sidewall spacers adjacent the sacrificial gate structures, forming a first metal layer adjacent said sidewall spacers, and planarizing the first metal layer.

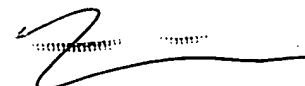
7. Claims 12, 14, and 15 are rejected under 35 USC 112, first paragraph, but would be allowable **(1)** if rewritten in independent form including all of the limitations of the base claim and any intervening claims, and **(2)** if rewritten to overcome the rejection under 35 U.S.C. 112, first paragraph set forth in this action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toniae M. Thomas whose telephone number is (571) 272-1846. The examiner can normally be reached on Monday through Friday from 8:30 a.m. to 5:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TMT
25 June 2005



Mary Wilczewski
Primary Examiner